

# 1Gb DDR3L SDRAM

*Lead-Free&Halogen-Free*

*(RoHS Compliant)*

**H5TC1G83EFR-xxA**

**H5TC1G83EFR-xxI**

**H5TC1G63EFR-xxA**

**H5TC1G63EFR-xxI**

*\*SK hynix Inc. reserves the right to change products or specifications without notice*

## Revision History

Revision No.	History	Date	Remark
1.0	Official Version Release	July. 2012	

## Description

The H5TC1G83EFR-xxA(I) and H5TC1G63EFR-xxA(I) are a 1Gb low power Double Data Rate III (DDR3L) Synchronous DRAM, ideally suited for the main memory applications which requires large memory density, high bandwidth and low power operation at 1.35V. SK Hynix DDR3L SDRAM provides backward compatibility with the 1.5V DDR3 based environment without any changes. (Please refer to the SPD information for details.)

SK Hynix 1Gb DDR3L SDRAMs offer fully synchronous operations referenced to both rising and falling edges of the clock. While all addresses and control inputs are latched on the rising edges of the clock (falling edges of the clock), data, data strobes and write data masks inputs are sampled on both rising and falling edges of it. The data paths are internally pipelined and 8-bit prefetched to achieve very high bandwidth.

## Device Features and Ordering Information

### FEATURES

- VDD=VDDQ=1.35V + 0.100 / - 0.067V
- Fully differential clock inputs (CK,  $\overline{\text{CK}}$ ) operation
- Differential Data Strobe (DQS,  $\overline{\text{DQS}}$ )
- On chip DLL align DQ, DQS and  $\overline{\text{DQS}}$  transition with CK transition
- DM masks write data-in at the both rising and falling edges of the data strobe
- All addresses and control inputs except data, data strobes and data masks latched on the rising edges of the clock
- Programmable CAS latency 6, 7, 8, 9, 10, 11, 12 and 13 supported
- Programmable additive latency 0, CL-1, and CL-2 supported
- Programmable CAS Write latency (CWL) = 5, 6, 7, 8
- Programmable burst length 4/8 with both nibble sequential and interleave mode
- BL switch on the fly
- 8banks
- Average Refresh Cycle (Tcase of 0 °C~95 °C)
  - 7.8  $\mu\text{s}$  at 0 °C ~ 85 °C
  - 3.9  $\mu\text{s}$  at 85 °C ~ 95 °C
- Commercial Temperature (0 °C ~ 85 °C)
- Industrial Temperature (-40 °C ~ 95 °C)
- JEDEC standard 78ball FBGA(x8), 96ball FBGA(x16)
- Driver strength selected by EMRS
- Dynamic On Die Termination supported
- Asynchronous RESET pin supported
- ZQ calibration supported
- TDQS (Termination Data Strobe) supported (x8 only)
- Write Levelization supported
- 8 bit pre-fetch

**\* This product in compliance with the RoHS directive.**

## ORDERING INFORMATION

Part No.	Configuration	Temperature	Package
H5TC1G83EFR-*xxA	128M x 8	Commercial	78ball FBGA
H5TC1G83EFR-*xxI		Industrial	
H5TC1G63EFR-*xxA	64M x 16	Commercial	96ball FBGA
H5TC1G63EFR-*xxI		Industrial	

\* xx means Speed Bin Grade

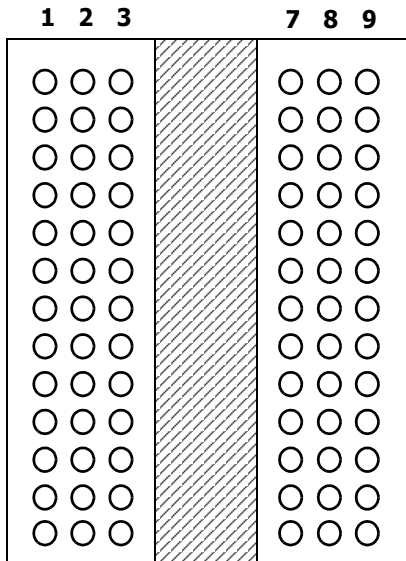
## OPERATING FREQUENCY

Speed Grade (Marking)	Frequency [MHz]										Remark (CL-tRCD-tRP)
	CL5	CL6	CL7	CL8	CL9	CL10	CL11	CL12	CL13	CL14	
-G7	667	800	1066	1066							DDR3L-1066 7-7-7
-H9	667	800	1066	1066	1333	1333					DDR3L-1333 9-9-9
-PB	667	800	1066	1066	1333	1333	1600				DDR3L-1600 11-11-11
-RD		800	1066	1066	1333	1333	1600		1866		DDR3L-1866 13-13-13

## Package Ballout/Mechanical Dimension

### x8 Package Ball out (Top view): 78ball FBGA Package (no support balls)

	1	2	3	4	5	6	7	8	9	
A	VSS	VDD	NC				NU/TDQS	VSS	VDD	A
B	VSS	VSSQ	DQ0				DM/TDQS	VSSQ	VDDQ	B
C	VDDQ	DQ2	DQS				DQ1	DQ3	VSSQ	C
D	VSSQ	DQ6	DQS				VDD	VSS	VSSQ	D
E	VREFDQ	VDDQ	DQ4				DQ7	DQ5	VDDQ	E
F	NC	VSS	RAS				CK	VSS	NC	F
G	ODT	VDD	CAS				CK	VDD	CKE	G
H	NC	CS	WE				A10/AP	ZQ	NC	H
J	VSS	BA0	BA2				NC	VREFCA	VSS	J
K	VDD	A3	A0				A12/BC	BA1	VDD	K
L	VSS	A5	A2				A1	A4	VSS	L
M	VDD	A7	A9				A11	A6	VDD	M
N	VSS	RESET	A13				NC	A8	VSS	N

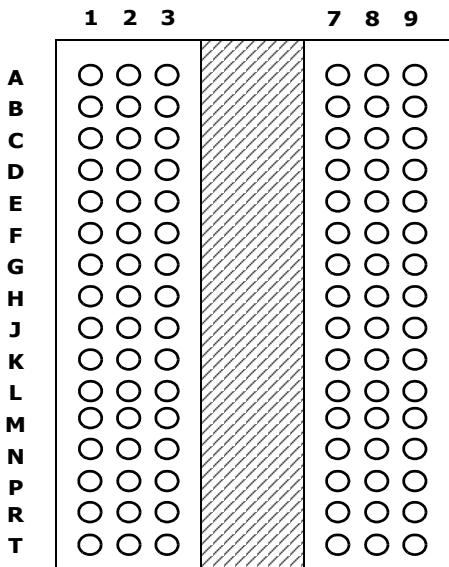


(Top View: See the balls through the Package)

- Populated ball
- + Ball not populated

### x16 Package Ball out (Top view): 96ball FBGA Package (no support balls)

	1	2	3	4	5	6	7	8	9	
A	VDDQ	DQU5	DQU7				DQU4	VDDQ	VSS	A
B	VSSQ	VDD	VSS				DQSU#	DQU6	VSSQ	B
C	VDDQ	DQU3	DQU1				DQSU	DQU2	VDDQ	C
D	VSSQ	VDDQ	DMU				DQU0	VSSQ	VDD	D
E	VSS	VSSQ	DQL0				DML	VSSQ	VDDQ	E
F	VDDQ	DQL2	DQSL				DQL1	DQL3	VSSQ	F
G	VSSQ	DQL6	DQSL#				VDD	VSS	VSSQ	G
H	VREFDQ	VDDQ	DQL4				DQL7	DQL5	VDDQ	H
J	NC	VSS	RAS#				CK	VSS	NC	J
K	ODT	VDD	CAS#				CK#	VDD	CKE	K
L	NC	CS#	WE#				A10/AP	ZQ	NC	L
M	VSS	BA0	BA2				NC	VREFCA	VSS	M
N	VDD	A3	A0				A12/BC#	BA1	VDD	N
P	VSS	A5	A2				A1	A4	VSS	P
R	VDD	A7	A9				A11	A6	VDD	R
T	VSS	RESET#	NC				NC	A8	VSS	T



(Top View: See the balls through the Package)

- Populated ball
- + Ball not populated

## Pin Functional Description

Symbol	Type	Function
CK, $\overline{CK}$	Input	Clock: CK and $\overline{CK}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of $\overline{CK}$ .
CKE, (CKE0), (CKE1)	Input	Clock Enable: CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is asynchronous for Self-Refresh exit. After VREFCA and VREFDQ have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, $\overline{CK}$ , ODT and CKE, are disabled during power-down. Input buffers, excluding CKE, are disabled during Self-Refresh.
$\overline{CS}$ , ( $\overline{CS0}$ ), ( $\overline{CS1}$ ), ( $\overline{CS2}$ ), ( $\overline{CS3}$ )	Input	Chip Select: All commands are masked when $\overline{CS}$ is registered HIGH. $\overline{CS}$ provides for external Rank selection on systems with multiple Ranks. $\overline{CS}$ is considered part of the command code.
ODT, (ODT0), (ODT1)	Input	On Die Termination: ODT (registered HIGH) enables termination resistance internal to the DDR3 SDRAM. When enabled, ODT is only applied to each DQ, DQS, $\overline{DQS}$ and DM/TDQS, NU/ $\overline{TDQS}$ (When TDQS is enabled via Mode Register A11=1 in MR1) signal for x8 configurations. For x16 configuration, ODT is applied to each DQ, DQSU, $\overline{DQSU}$ , DQSL, $\overline{DQSL}$ , DMU, and DML signal. The ODT pin will be ignored if MR1 is programmed to disable ODT.
$\overline{RAS}$ , $\overline{CAS}$ , $\overline{WE}$	Input	Command Inputs: $\overline{RAS}$ , $\overline{CAS}$ and $\overline{WE}$ (along with $\overline{CS}$ ) define the command being entered.
DM, (DMU), (DML)	Input	Input Data Mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of DQS. For x8 device, the function of DM or TDQS/TDQS is enabled by Mode Register A11 setting in MR1.
BA0 - BA2	Input	Bank Address Inputs: BA0 - BA2 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines if the mode register or extended mode register is to be accessed during a MRS cycle.
A0 - A15	Input	Address Inputs: Provide the row address for Active commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. (A10/AP and A12/ $\overline{BC}$ have additional functions, see below). The address inputs also provide the op-code during Mode Register Set commands.
A10 / AP	Input	Auto-precharge: A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: no Autoprecharge). A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses.
A12 / $\overline{BC}$	Input	Burst Chop: A12 / $\overline{BC}$ is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See command truth table for details.

Symbol	Type	Function
$\overline{\text{RESET}}$	Input	Active Low Asynchronous Reset: Reset is active when $\overline{\text{RESET}}$ is LOW, and inactive when $\overline{\text{RESET}}$ is HIGH. $\overline{\text{RESET}}$ must be HIGH during normal operation. $\overline{\text{RESET}}$ is a CMOS rail-to-rail signal with DC high and low at 80% and 20% of $V_{DD}$ , i.e. 1.20V for DC high and 0.30V for DC low.
DQ	Input / Output	Data Input/ Output: Bi-directional data bus.
DQU, DQL, DQS, $\overline{\text{DQS}}$ , DQSU, $\overline{\text{DQSU}}$ , DQSL, $\overline{\text{DQSL}}$	Input / Output	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. The data strobe DQS, DQSL, and DQSU are paired with differential signals $\overline{\text{DQS}}$ , $\overline{\text{DQSL}}$ , and $\overline{\text{DQSU}}$ , respectively, to provide differential pair signaling to the system during reads and writes. DDR3 SDRAM supports differential data strobe only and does not support single-ended.
TDQS, $\overline{\text{TDQS}}$	Output	Termination Data Strobe: TDQS/ $\overline{\text{TDQS}}$ is applicable for x8 DRAMs only. When enabled via Mode Register A11 = 1 in MR1, the DRAM will enable the same termination resistance function on TDQS/ $\overline{\text{TDQS}}$ that is applied to DQS/ $\overline{\text{DQS}}$ . When disabled via mode register A11 = 0 in MR1, DM/ $\overline{\text{DM}}$ will provide the data mask function and $\overline{\text{TDQS}}$ is not used. x16 DRAMs must disable the TDQS function via mode register A11 = 0 in MR1.
NC		No Connect: No internal electrical connection is present.
NF		No Function
$V_{DDQ}$	Supply	DQ Power Supply: 1.5 V +/- 0.075 V
$V_{SSQ}$	Supply	DQ Ground
$V_{DD}$	Supply	Power Supply: 1.5 V +/- 0.075 V
$V_{SS}$	Supply	Ground
$V_{REFDQ}$	Supply	Reference voltage for DQ
$V_{REFCA}$	Supply	Reference voltage for CA
ZQ	Supply	Reference Pin for ZQ calibration

**Note:**

Input only pins (BA0-BA2, A0-A15,  $\overline{\text{RAS}}$ ,  $\overline{\text{CAS}}$ ,  $\overline{\text{WE}}$ ,  $\overline{\text{CS}}$ , CKE, ODT, DM, and  $\overline{\text{RESET}}$ ) do not supply termination.



## ROW AND COLUMN ADDRESS TABLE

### 1Gb

Configuration	128Mb x 8	64Mb x 16
# of Banks	8	8
Bank Address	BA0 - BA2	BA0 - BA2
Auto precharge	A10/AP	A10/AP
BL switch on the fly	A12/BC	A12/BC
Row Address	A0 - A13	A0 - A12
Column Address	A0 - A9	A0 - A9
Page size <sup>1</sup>	1 KB	2 KB

**Note1:** Page size is the number of bytes of data delivered from the array to the internal sense amplifiers when an ACTIVE command is registered. Page size is per bank, calculated as follows:

$$\text{page size} = 2^{\text{COLBITS}} * \text{ORG} \div 8$$

where COLBITS = the number of column address bits, ORG = the number of I/O (DQ) bits

## Absolute Maximum Ratings

### Absolute Maximum DC Ratings

#### Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Units	Notes
VDD	Voltage on VDD pin relative to Vss	- 0.4 V ~ 1.975 V	V	1,3
VDDQ	Voltage on VDDQ pin relative to Vss	- 0.4 V ~ 1.975 V	V	1,3
V <sub>IN</sub> , V <sub>OUT</sub>	Voltage on any pin relative to Vss	- 0.4 V ~ 1.975 V	V	1
T <sub>STG</sub>	Storage Temperature	-55 to +100	°C	1, 2

#### Notes:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JEDEC standard.
3. VDD and VDDQ must be within 300mV of each other at all times; and VREF must not be greater than 0.6XVDDQ, When VDD and VDDQ are less than 500mV; VREF may be equal to or less than 300mV.

## DRAM Component Operating Temperature Range

### Temperature Range

Symbol	Parameter	Rating	Units	Notes
T <sub>OPER</sub>	Normal Operating Temperature Range	0 to 85	°C	1,2
	Industrial Temperature Range	-40 to 95	°C	1,3

#### Notes:

1. Operating Temperature T<sub>OPER</sub> is the case surface temperature on the center / top side of the DRAM. For measurement conditions, please refer to the JEDEC document JEDEC51-2.
2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0 - 85°C under all operating conditions.
3. Some applications require operation of the DRAM in the Extended Temperature Range between 85°C and 95°C case temperature. Full specifications are guaranteed in this range, but the following additional conditions apply:
  - a. Refresh commands must be doubled in frequency, therefore reducing the Refresh interval tREFI to 3.9 μs.
  - b. If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 = 0b and MR2 A7 = 1b).

## AC & DC Operating Conditions

### Recommended DC Operating Conditions

#### Recommended DC Operating Conditions - DDR3L (1.35V) operation

Symbol	Parameter	Rating			Units	Notes
		Min.	Typ.	Max.		
VDD	Supply Voltage	1.283	1.35	1.45	V	1,2,3,4
VDDQ	Supply Voltage for Output	1.283	1.35	1.45	V	1,2,3,4

**Notes:**

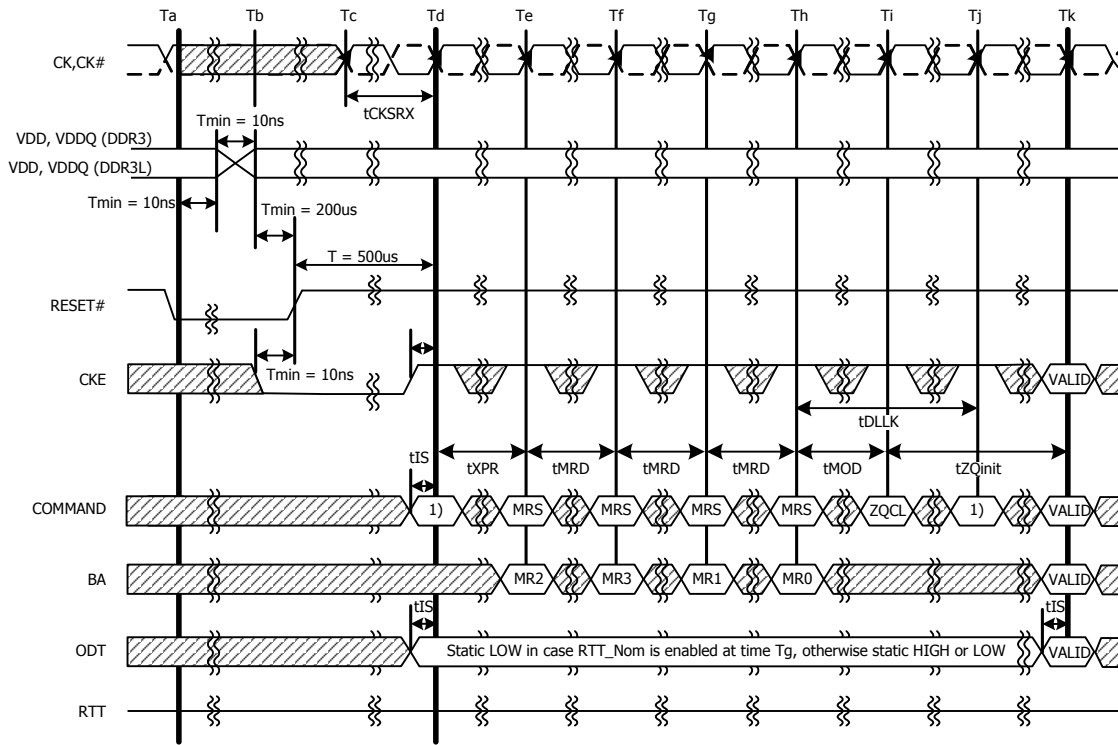
1. Maximum DC value may not be greater than 1.425V. The DC value is the linear average of VDD/VDDQ (t) over a very long period of time (e.g., 1 sec).
2. If maximum limit is exceeded, input levels shall be governed by DDR3 specifications.
3. Under these supply voltages, the device operates to this DDR3L specification.
4. Once initialized for DDR3L operation, DDR3 operation may only be used if the device is in reset while VDD and VDDQ are changed for DDR3 operation (see Figure 0).

#### Recommended DC Operating Conditions - DDR3 (1.5V) operation

Symbol	Parameter	Rating			Units	Notes
		Min.	Typ.	Max.		
VDD	Supply Voltage	1.425	1.5	1.575	V	1,2,3
VDDQ	Supply Voltage for Output	1.425	1.5	1.575	V	1,2,3

**Notes:**

1. If minimum limit is exceeded, input levels shall be governed by DDR3L specifications.
2. Under 1.5V operation, this DDR3L device operates to the DDR3 specifications under the same speed timings as defined for this device.
3. Once initialized for DDR3 operation, DDR3L operation may only be used if the device is in reset while VDD and VDDQ are changed for DDR3L operation (see Figure 0).



NOTE 1: From time point "Td" until "Tk" NOP or DES commands must be applied between MRS and ZQCL commands.

|| TIME BREAK    ▨ DON'T CARE

Figure 0 - VDD/VDDQ Voltage Switch Between DDR3L and DDR3

## IDD and IDDQ Specification Parameters and Test Conditions

### IDD and IDDQ Measurement Conditions

In this chapter, IDD and IDDQ measurement conditions such as test load and patterns are defined. Figure 1. shows the setup and test load for IDD and IDDQ measurements.

- IDD currents (such as IDD0, IDD1, IDD2N, IDD2NT, IDD2P0, IDD2P1, IDD2Q, IDD3N, IDD3P, IDD4R, IDD4W, IDD5B, IDD6, IDD6ET, and IDD7) are measured as time-averaged currents with all VDD balls of the DDR3 SDRAM under test tied together. Any IDDQ current is not included in IDD currents.
- IDDQ currents (such as IDDQ2NT and IDDQ4R) are measured as time-averaged currents with all VDDQ balls of the DDR3 SDRAM under test tied together. Any IDD current is not included in IDDQ currents.

Attention: IDDQ values cannot be directly used to calculate IO power of the DDR3 SDRAM. They can be used to support correlation of simulated IO power to actual IO power as outlined in Figure 2. In DRAM module application, IDDQ cannot be measured separately since VDD and VDDQ are using one merged-power layer in Module PCB.

For IDD and IDDQ measurements, the following definitions apply:

- "0" and "LOW" is defined as  $V_{IN} \leq V_{ILAC(max)}$ .
- "1" and "HIGH" is defined as  $V_{IN} \geq V_{IHAC(min)}$ .
- "MID\_LEVEL" is defined as inputs are  $V_{REF} = VDD/2$ .
- Timing used for IDD and IDDQ Measurement-Loop Patterns are provided in Table 1.
- Basic IDD and IDDQ Measurement Conditions are described in Table 2.
- Detailed IDD and IDDQ Measurement-Loop Patterns are described in Table 3 through Table 10.
- IDD Measurements are done after properly initializing the DDR3 SDRAM. This includes but is not limited to setting  
 $R_{ON} = RZQ/7$  (34 Ohm in MR1);  
 $Q_{off} = 0_B$  (Output Buffer enabled in MR1);  
 $R_{TT\_Nom} = RZQ/6$  (40 Ohm in MR1);  
 $R_{TT\_Wr} = RZQ/2$  (120 Ohm in MR2);  
 TDQS Feature disabled in MR1
- Attention: The IDD and IDDQ Measurement-Loop Patterns need to be executed at least one time before actual IDD or IDDQ measurement is started.
- Define  $D = \{\overline{CS}, \overline{RAS}, \overline{CAS}, \overline{WE}\} := \{HIGH, LOW, LOW, LOW\}$
- Define  $\overline{D} = \{\overline{CS}, \overline{RAS}, \overline{CAS}, \overline{WE}\} := \{HIGH, HIGH, HIGH, HIGH\}$

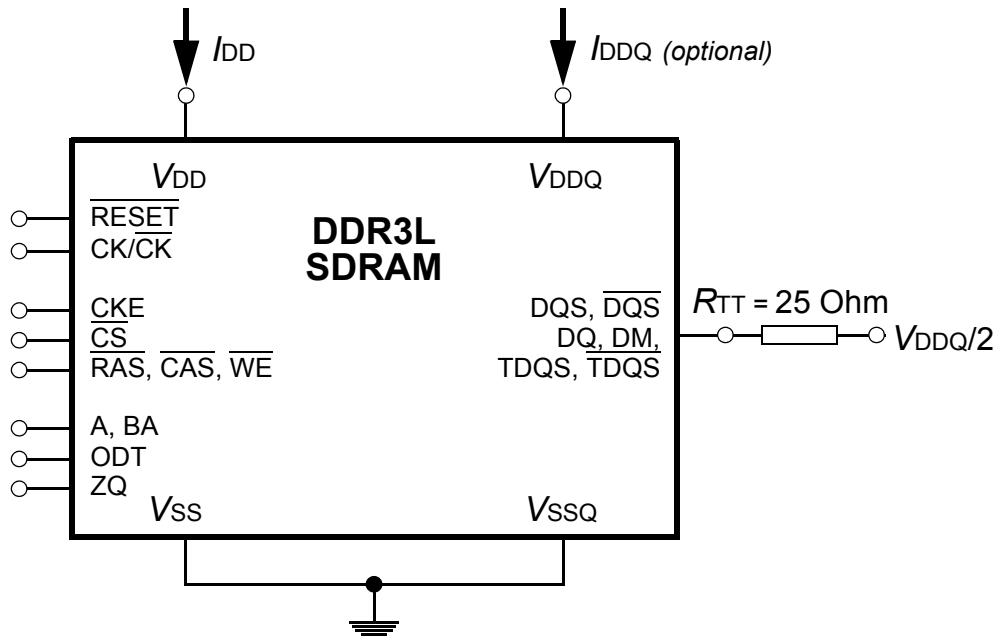


Figure 1 - Measurement Setup and Test Load for IDD and IDDQ (optional) Measurements  
 [Note: DIMM level Output test load condition may be different from above]

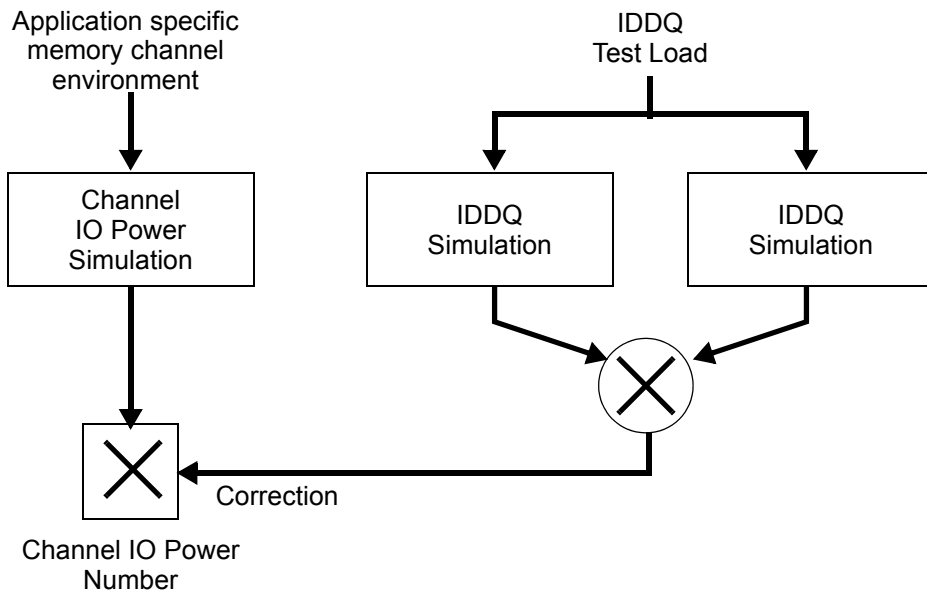


Figure 2 - Correlation from simulated Channel IO Power to actual Channel IO Power supported by IDDQ Measurement

**Table 1 -Timings used for IDD and IDDQ Measurement-Loop Patterns**

Symbol	DDR3L-1066	DDR3L-1333	DDR3L-1600	DDR3L-1866	Unit
	7-7-7	9-9-9	11-11-11	13-13-13	
$t_{CK}$	1.875	1.5	1.25	1.07	ns
CL	7	9	11	13	nCK
$t_{RCD}$	7	9	11	13	nCK
$t_{RC}$	27	33	39	45	nCK
$t_{RAS}$	20	24	28	32	nCK
$t_{RP}$	7	9	11	13	nCK
$t_{FAW}$	1KB page size	20	20	24	nCK
	2KB page size	27	30	32	nCK
$t_{RRD}$	1KB page size	4	4	5	nCK
	2KB page size	6	5	6	nCK
$t_{RFC}$ -512Mb	48	60	72	85	nCK
$t_{RFC}$ -1 Gb	59	74	88	103	nCK
$t_{RFC}$ -2 Gb	86	107	128	150	nCK
$t_{RFC}$ -4 Gb	160	200	240	281	nCK
$t_{RFC}$ -8 Gb	187	234	280	328	nCK

**Table 2 -Basic IDD and IDDQ Measurement Conditions**

Symbol	Description
$I_{DD0}$	<p>Operating One Bank Active-Precharge Current</p> <p>CKE: High; External clock: On; <math>t_{CK}</math>, nRC, nRAS, CL: see Table 1; BL: 8<sup>a</sup>); AL: 0; <math>\overline{CS}</math>: High between ACT and PRE; Command, Address, Bank Address Inputs: partially toggling according to Table 3; Data IO: MID-LEVEL; DM: stable at 0; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,... (see Table 3); Output Buffer and RTT: Enabled in Mode Registers<sup>b</sup>); ODT Signal: stable at 0; Pattern Details: see Table 3.</p>
$I_{DD1}$	<p>Operating One Bank Active-Read-Precharge Current</p> <p>CKE: High; External clock: On; <math>t_{CK}</math>, nRC, nRAS, nRCD, CL: see Table 1; BL: 8<sup>a</sup>); AL: 0; <math>\overline{CS}</math>: High between ACT, RD and PRE; Command, Address; Bank Address Inputs, Data IO: partially toggling according to Table 4; DM: stable at 0; Bank Activity: Cycling with on bank active at a time: 0,0,1,1,2,2,... (see Table 4); Output Buffer and RTT: Enabled in Mode Registers<sup>b</sup>); ODT Signal: stable at 0; Pattern Details: see Table 4.</p>

Symbol	Description
$I_{DD2N}$	Precharge Standby Current CKE: High; External clock: On; tCK, CL: see Table 1; BL: 8 <sup>a)</sup> ; AL: 0; $\overline{CS}$ : stable at 1; Command, Address, Bank Address Inputs: partially toggling according to Table 5; Data IO: MID-LEVEL; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers <sup>b)</sup> ; ODT Signal: stable at 0; Pattern Details: see Table 5.
$I_{DD2NT}$	Precharge Standby ODT Current CKE: High; External clock: On; tCK, CL: see Table 1; BL: 8 <sup>a)</sup> ; AL: 0; $\overline{CS}$ : stable at 1; Command, Address, Bank Address Inputs: partially toggling according to Table 6; Data IO: MID-LEVEL; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers <sup>b)</sup> ; ODT Signal: toggling according to Table 6; Pattern Details: see Table 6.
$I_{DD2PO}$	Precharge Power-Down Current Slow Exit CKE: Low; External clock: On; tCK, CL: see Table 1; BL: 8 <sup>a)</sup> ; AL: 0; $\overline{CS}$ : stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO: MID-LEVEL; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers <sup>b)</sup> ; ODT Signal: stable at 0; Precharge Power Down Mode: Slow Exit <sup>c)</sup>
$I_{DD2P1}$	Precharge Power-Down Current Fast Exit CKE: Low; External clock: On; tCK, CL: see Table 1; BL: 8 <sup>a)</sup> ; AL: 0; $\overline{CS}$ : stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO: MID-LEVEL; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers <sup>b)</sup> ; ODT Signal: stable at 0; Precharge Power Down Mode: Fast Exit <sup>c)</sup>
$I_{DD2Q}$	Precharge Quiet Standby Current CKE: High; External clock: On; tCK, CL: see Table 1; BL: 8 <sup>a)</sup> ; AL: 0; $\overline{CS}$ : stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO: MID-LEVEL; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers <sup>b)</sup> ; ODT Signal: stable at 0
$I_{DD3N}$	Active Standby Current CKE: High; External clock: On; tCK, CL: see Table 1; BL: 8 <sup>a)</sup> ; AL: 0; $\overline{CS}$ : stable at 1; Command, Address, Bank Address Inputs: partially toggling according to Table 5; Data IO: MID-LEVEL; DM: stable at 0; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers <sup>b)</sup> ; ODT Signal: stable at 0; Pattern Details: see Table 5.



Symbol	Description
$I_{DD3P}$	Active Power-Down Current CKE: Low; External clock: On; tCK, CL: see Table 1; BL: 8 <sup>a)</sup> ; AL: 0; $\overline{CS}$ : stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO: MID-LEVEL; DM: stable at 0; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers <sup>b)</sup> ; ODT Signal: stable at 0
$I_{DD4R}$	Operating Burst Read Current CKE: High; External clock: On; tCK, CL: see Table 1; BL: 8 <sup>a)</sup> ; AL: 0; $\overline{CS}$ : High between RD; Command, Address, Bank Address Inputs: partially toggling according to Table 7; Data IO: seamless read data burst with different data between one burst and the next one according to Table 7; DM: stable at 0; Bank Activity: all banks open, RD commands cycling through banks: 0,0,1,1,2,2,...(see Table 7); Output Buffer and RTT: Enabled in Mode Registers <sup>b)</sup> ; ODT Signal: stable at 0; Pattern Details: see Table 7.
$I_{DD4W}$	Operating Burst Write Current CKE: High; External clock: On; tCK, CL: see Table 1; BL: 8 <sup>a)</sup> ; AL: 0; $\overline{CS}$ : High between WR; Command, Address, Bank Address Inputs: partially toggling according to Table 8; Data IO: seamless read data burst with different data between one burst and the next one according to Table 8; DM: stable at 0; Bank Activity: all banks open, WR commands cycling through banks: 0,0,1,1,2,2,...(see Table 8); Output Buffer and RTT: Enabled in Mode Registers <sup>b)</sup> ; ODT Signal: stable at HIGH; Pattern Details: see Table 8.
$I_{DD5B}$	Burst Refresh Current CKE: High; External clock: On; tCK, CL, nRFC: see Table 1; BL: 8 <sup>a)</sup> ; AL: 0; $\overline{CS}$ : High between REF; Command, Address, Bank Address Inputs: partially toggling according to Table 9; Data IO: MID-LEVEL; DM: stable at 0; Bank Activity: REF command every nREC (see Table 9); Output Buffer and RTT: Enabled in Mode Registers <sup>b)</sup> ; ODT Signal: stable at 0; Pattern Details: see Table 9.
$I_{DD6}$	Self-Refresh Current: Normal Temperature Range $T_{CASE}$ : 0 - 85 °C; Auto Self-Refresh (ASR): Disabled <sup>d)</sup> ; Self-Refresh Temperature Range (SRT): Normal <sup>e)</sup> ; CKE: Low; External clock: Off; CK and $\overline{CK}$ : LOW; CL: see Table 1; BL: 8 <sup>a)</sup> ; AL: 0; $\overline{CS}$ , Command, Address, Bank Address Inputs, Data IO: MID-LEVEL; DM: stable at 0; Bank Activity: Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers <sup>b)</sup> ; ODT Signal: MID-LEVEL
$I_{DD6ET}$	Self-Refresh Current: Extended Temperature Range $T_{CASE}$ : 0 - 95 °C; Auto Self-Refresh (ASR): Disabled <sup>d)</sup> ; Self-Refresh Temperature Range (SRT): Extended <sup>e)</sup> ; CKE: Low; External clock: Off; CK and $\overline{CK}$ : LOW; CL: see Table 1; BL: 8 <sup>a)</sup> ; AL: 0; $\overline{CS}$ , Command, Address, Bank Address Inputs, Data IO: MID-LEVEL; DM: stable at 0; Bank Activity: Extended Temperature Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers <sup>b)</sup> ; ODT Signal: MID-LEVEL

Symbol	Description
<b><math>I_{DD7}</math></b>	Operating Bank Interleave Read Current CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, NRRD, nFAW, CL: see Table 1; BL: 8 <sup>a)f)</sup> ; AL: CL-1; $\overline{CS}$ : High between ACT and RDA; Command, Address, Bank Address Inputs: partially toggling according to Table 10; Data IO: read data burst with different data between one burst and the next one according to Table 10; DM: stable at 0; Bank Activity: two times interleaved cycling through banks (0, 1,...7) with different addressing, see Table 10; Output Buffer and RTT: Enabled in Mode Registers <sup>b)</sup> ; ODT Signal: stable at 0; Pattern Details: see Table 10.

a) Burst Length: BL8 fixed by MRS: set MR0 A[1,0]=00B

b) Output Buffer Enable: set MR1 A[12] = 0B; set MR1 A[5,1] = 01B; RTT\_Nom enable: set MR1 A[9,6,2] = 011B;  
 RTT\_Wr enable: set MR2 A[10,9] = 10B

c) Precharge Power Down Mode: set MR0 A12=0B for Slow Exit or MR0 A12 = 1B for Fast Exit

d) Auto Self-Refresh (ASR): set MR2 A6 = 0B to disable or 1B to enable feature

e) Self-Refresh Temperature Range (SRT): set MR2 A7 = 0B for normal or 1B for extended temperature range

f) Read Burst Type: Nibble Sequential, set MR0 A[3] = 0B

**Table 3 - IDD0 Measurement-Loop Pattern<sup>a)</sup>**

$\overline{\text{CK}}$ , CK	CKE	Sub-Loop	Cycle Number	Command	$\overline{\text{CS}}$	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data <sup>b)</sup>		
toggling	Static High	0	0	ACT	0	0	1	1	0	0	00	0	0	0	0	-		
			1,2	D, D	1	0	0	0	0	0	0	00	0	0	0	0	-	
			3,4	$\overline{\text{D}}, \overline{\text{D}}$	1	1	1	1	0	0	0	00	0	0	0	0	-	
			...	repeat pattern 1...4 until nRAS - 1, truncate if necessary														
			nRAS	PRE	0	0	1	0	0	0	0	00	0	0	0	0	-	
			...	repeat pattern 1...4 until nRC - 1, truncate if necessary														
			1*nRC+0	ACT	0	0	1	1	0	0	0	00	0	0	F	0	-	
			1*nRC+1, 2	D, D	1	0	0	0	0	0	0	00	0	0	F	0	-	
			1*nRC+3, 4	$\overline{\text{D}}, \overline{\text{D}}$	1	1	1	1	0	0	0	00	0	0	F	0	-	
			...	repeat pattern nRC+1...4 until 1*nRC + nRAS - 1, truncate if necessary														
			1*nRC+nRAS	PRE	0	0	1	0	0	0	0	00	0	0	F	0	-	
			...	repeat pattern nRC+1...4 until 2*nRC - 1, truncate if necessary														
			1	2*nRC	repeat Sub-Loop 0, use BA[2:0] = 1 instead													
			2	4*nRC	repeat Sub-Loop 0, use BA[2:0] = 2 instead													
			3	6*nRC	repeat Sub-Loop 0, use BA[2:0] = 3 instead													
			4	8*nRC	repeat Sub-Loop 0, use BA[2:0] = 4 instead													
			5	10*nRC	repeat Sub-Loop 0, use BA[2:0] = 5 instead													
	6	12*nRC	repeat Sub-Loop 0, use BA[2:0] = 6 instead															
	7	14*nRC	repeat Sub-Loop 0, use BA[2:0] = 7 instead															

a) DM must be driven LOW all the time. DQS,  $\overline{\text{DQS}}$  are MID-LEVEL.

b) DQ signals are MID-LEVEL.

**Table 4 - IDD1 Measurement-Loop Pattern<sup>a)</sup>**

CK, CK	CKE	Sub-Loop	Cycle Number	Command	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data <sup>b)</sup>		
toggling	Static High	0	0	ACT	0	0	1	1	0	0	00	0	0	0	0	-		
			1,2	D, D	1	0	0	0	0	0	0	00	0	0	0	0	-	
			3,4	$\overline{D}$ , $\overline{D}$	1	1	1	1	1	0	0	00	0	0	0	0	0	-
			...	repeat pattern 1...4 until nRCD - 1, truncate if necessary														
			nRCD	RD	0	1	0	1	0	0	0	00	0	0	0	0	0	00000000
			...	repeat pattern 1...4 until nRAS - 1, truncate if necessary														
			nRAS	PRE	0	0	1	0	0	0	0	00	0	0	0	0	0	-
			...	repeat pattern 1...4 until nRC - 1, truncate if necessary														
			1*nRC+0	ACT	0	0	1	1	0	0	0	00	0	0	F	0	0	-
			1*nRC+1,2	D, D	1	0	0	0	0	0	0	00	0	0	F	0	0	-
			1*nRC+3,4	$\overline{D}$ , $\overline{D}$	1	1	1	1	0	0	0	00	0	0	F	0	0	-
			...	repeat pattern nRC + 1,...4 until nRC + nRCD - 1, truncate if necessary														
			1*nRC+nRCD	RD	0	1	0	1	0	0	0	00	0	0	F	0	0	00110011
			...	repeat pattern nRC + 1,...4 until nRC + nRAS - 1, truncate if necessary														
			1*nRC+nRAS	PRE	0	0	1	0	0	0	0	00	0	0	F	0	0	-
			...	repeat pattern nRC + 1,...4 until 2* nRC - 1, truncate if necessary														
			1	2*nRC	repeat Sub-Loop 0, use BA[2:0] = 1 instead													
			2	4*nRC	repeat Sub-Loop 0, use BA[2:0] = 2 instead													
			3	6*nRC	repeat Sub-Loop 0, use BA[2:0] = 3 instead													
			4	8*nRC	repeat Sub-Loop 0, use BA[2:0] = 4 instead													
	5	10*nRC	repeat Sub-Loop 0, use BA[2:0] = 5 instead															
	6	12*nRC	repeat Sub-Loop 0, use BA[2:0] = 6 instead															
	7	14*nRC	repeat Sub-Loop 0, use BA[2:0] = 7 instead															

a) DM must be driven LOW all the time. DQS,  $\overline{DQS}$  are used according to RD Commands, otherwise MID-LEVEL.

b) Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are MID-LEVEL.

**Table 5 - IDD2N and IDD3N Measurement-Loop Pattern<sup>a)</sup>**

CK, $\overline{\text{CK}}$	CKE	Sub-Loop	Cycle Number	Command	$\overline{\text{CS}}$	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data <sup>b)</sup>		
toggling	Static High	0	0	D	1	0	0	0	0	0	0	0	0	0	0	-		
			1	D	1	0	0	0	0	0	0	0	0	0	0	0	-	
			2	$\overline{\text{D}}$	1	1	1	1	0	0	0	0	0	0	F	0	-	
			3	$\overline{\text{D}}$	1	1	1	1	0	0	0	0	0	0	F	0	-	
		1	4-7	repeat Sub-Loop 0, use BA[2:0] = 1 instead														
		2	8-11	repeat Sub-Loop 0, use BA[2:0] = 2 instead														
		3	12-15	repeat Sub-Loop 0, use BA[2:0] = 3 instead														
		4	16-19	repeat Sub-Loop 0, use BA[2:0] = 4 instead														
		5	20-23	repeat Sub-Loop 0, use BA[2:0] = 5 instead														
		6	24-27	repeat Sub-Loop 0, use BA[2:0] = 6 instead														
		7	28-31	repeat Sub-Loop 0, use BA[2:0] = 7 instead														

a) DM must be driven LOW all the time. DQS,  $\overline{\text{DQS}}$  are MID-LEVEL.

b) DQ signals are MID-LEVEL.

**Table 6 - IDD2NT and IDDQ2NT Measurement-Loop Pattern<sup>a)</sup>**

CK, $\overline{\text{CK}}$	CKE	Sub-Loop	Cycle Number	Command	$\overline{\text{CS}}$	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data <sup>b)</sup>		
toggling	Static High	0	0	D	1	0	0	0	0	0	0	0	0	0	0	-		
			1	D	1	0	0	0	0	0	0	0	0	0	0	0	-	
			2	$\overline{\text{D}}$	1	1	1	1	0	0	0	0	0	0	F	0	-	
			3	$\overline{\text{D}}$	1	1	1	1	0	0	0	0	0	0	F	0	-	
		1	4-7	repeat Sub-Loop 0, but ODT = 0 and BA[2:0] = 1														
		2	8-11	repeat Sub-Loop 0, but ODT = 1 and BA[2:0] = 2														
		3	12-15	repeat Sub-Loop 0, but ODT = 1 and BA[2:0] = 3														
		4	16-19	repeat Sub-Loop 0, but ODT = 0 and BA[2:0] = 4														
		5	20-23	repeat Sub-Loop 0, but ODT = 0 and BA[2:0] = 5														
		6	24-27	repeat Sub-Loop 0, but ODT = 1 and BA[2:0] = 6														
		7	28-31	repeat Sub-Loop 0, but ODT = 1 and BA[2:0] = 7														

a) DM must be driven LOW all the time. DQS,  $\overline{\text{DQS}}$  are MID-LEVEL.

b) DQ signals are MID-LEVEL.

**Table 7 - IDD4R and IDDQ4R Measurement-Loop Pattern<sup>a)</sup>**

$\overline{\text{CK}}$ , $\overline{\text{CK}}$	$\overline{\text{CKE}}$	Sub-Loop	Cycle Number	Command	$\overline{\text{CS}}$	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data <sup>b)</sup>		
toggling	Static High	0	0	RD	0	1	0	1	0	0	00	0	0	0	0	00000000		
			1	D	1	0	0	0	0	0	00	0	0	0	0	-		
			2,3	$\overline{\text{D}}, \overline{\text{D}}$	1	1	1	1	0	0	00	0	0	0	0	-		
			4	RD	0	1	0	1	0	0	00	0	0	F	0	00110011		
		5	D	1	0	0	0	0	0	0	00	0	0	F	0	-		
			$\overline{\text{D}}, \overline{\text{D}}$	1	1	1	1	0	0	00	0	0	F	0	-			
			repeat Sub-Loop 0, but BA[2:0] = 1															
		6	repeat Sub-Loop 0, but BA[2:0] = 2															
			repeat Sub-Loop 0, but BA[2:0] = 3															
			repeat Sub-Loop 0, but BA[2:0] = 4															
			repeat Sub-Loop 0, but BA[2:0] = 5															
		repeat Sub-Loop 0, but BA[2:0] = 6																
		repeat Sub-Loop 0, but BA[2:0] = 7																

a) DM must be driven LOW all the time. DQS,  $\overline{\text{DQS}}$  are used according to RD Commands, otherwise MID-LEVEL.

b) Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are MID-LEVEL.

**Table 8 - IDD4W Measurement-Loop Pattern<sup>a)</sup>**

CK, CK	CKE	Sub-Loop	Cycle Number	Command	CS	RAS	CAS	WE	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data <sup>b)</sup>		
toggling	Static High	0	0	WR	0	1	0	0	1	0	00	0	0	0	0	00000000		
			1	D	1	0	0	0	1	0	00	0	0	0	0	-		
			2,3	$\overline{D}, \overline{D}$	1	1	1	1	1	0	00	0	0	0	0	-		
			4	WR	0	1	0	0	0	1	0	00	0	0	F	0	00110011	
		5	D	1	0	0	0	0	1	0	00	0	0	F	0	-		
			6,7	$\overline{D}, \overline{D}$	1	1	1	1	1	0	00	0	0	F	0	-		
		1	8-15	repeat Sub-Loop 0, but BA[2:0] = 1														
		2	16-23	repeat Sub-Loop 0, but BA[2:0] = 2														
		3	24-31	repeat Sub-Loop 0, but BA[2:0] = 3														
		4	32-39	repeat Sub-Loop 0, but BA[2:0] = 4														
		5	40-47	repeat Sub-Loop 0, but BA[2:0] = 5														
		6	48-55	repeat Sub-Loop 0, but BA[2:0] = 6														
		7	56-63	repeat Sub-Loop 0, but BA[2:0] = 7														

a) DM must be driven LOW all the time. DQS,  $\overline{DQS}$  are used according to WR Commands, otherwise MID-LEVEL.

b) Burst Sequence driven on each DQ signal by Write Command. Outside burst operation, DQ signals are MID-LEVEL.

**Table 9 - IDD5B Measurement-Loop Pattern<sup>a)</sup>**

CK, CK	CKE	Sub-Loop	Cycle Number	Command	CS	RAS	CAS	WE	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data <sup>b)</sup>		
toggling	Static High	1	0	REF	0	0	0	1	0	0	0	0	0	0	0	-		
			1,2	D, D	1	0	0	0	0	0	0	00	0	0	0	0	-	
			3,4	$\overline{D}, \overline{D}$	1	1	1	1	1	0	0	00	0	0	F	0	-	
			5...8	repeat cycles 1...4, but BA[2:0] = 1														
			9...12	repeat cycles 1...4, but BA[2:0] = 2														
			13...16	repeat cycles 1...4, but BA[2:0] = 3														
			17...20	repeat cycles 1...4, but BA[2:0] = 4														
			21...24	repeat cycles 1...4, but BA[2:0] = 5														
			25...28	repeat cycles 1...4, but BA[2:0] = 6														
			29...32	repeat cycles 1...4, but BA[2:0] = 7														
		2	33...nRFC-1	repeat Sub-Loop 1, until nRFC - 1. Truncate, if necessary.														

a) DM must be driven LOW all the time. DQS,  $\overline{DQS}$  are MID-LEVEL.

b) DQ signals are MID-LEVEL.

**Table 10 - IDD7 Measurement-Loop Pattern<sup>a)</sup>**

ATTENTION! Sub-Loops 10-19 have inverse A[6:3] Pattern and Data Pattern than Sub-Loops 0-9

CK, CK	CKE	Sub-Loop	Cycle Number	Command	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data <sup>b)</sup>		
toggling	Static High	0	0	ACT	0	0	1	1	0	0	00	0	0	0	0	-		
			1	RDA	0	1	0	1	0	0	00	1	0	0	0	00000000		
			2	D	1	0	0	0	0	0	0	00	0	0	0	0	-	
			...	repeat above D Command until nRRD - 1														
		1	nRRD	ACT	0	0	1	1	0	1	00	0	0	F	0	-		
			nRRD+1	RDA	0	1	0	1	0	1	00	1	0	F	0	00110011		
			nRRD+2	D	1	0	0	0	0	0	1	00	0	0	F	0	-	
			...	repeat above D Command until 2* nRRD - 1														
		2	2*nRRD	repeat Sub-Loop 0, but BA[2:0] = 2														
		3	3*nRRD	repeat Sub-Loop 1, but BA[2:0] = 3														
		4	4*nRRD	D	1	0	0	0	0	0	3	00	0	0	F	0	-	
				Assert and repeat above D Command until nFAW - 1, if necessary														
		5	nFAW	repeat Sub-Loop 0, but BA[2:0] = 4														
		6	nFAW+nRRD	repeat Sub-Loop 1, but BA[2:0] = 5														
		7	nFAW+2*nRRD	repeat Sub-Loop 0, but BA[2:0] = 6														
		8	nFAW+3*nRRD	repeat Sub-Loop 1, but BA[2:0] = 7														
		9	nFAW+4*nRRD	D	1	0	0	0	0	0	7	00	0	0	F	0	-	
				Assert and repeat above D Command until 2* nFAW - 1, if necessary														
		10	2*nFAW+0	ACT	0	0	1	1	0	0	00	0	0	F	0	-		
				RDA	0	1	0	1	0	0	00	1	0	F	0	00110011		
				D	1	0	0	0	0	0	0	00	0	0	F	0	-	
			...	Repeat above D Command until 2* nFAW + nRRD - 1														
		11	2*nFAW+nRRD	ACT	0	0	1	1	0	1	00	0	0	0	0	-		
				RDA	0	1	0	1	0	1	00	1	0	0	0	00000000		
				D	1	0	0	0	0	0	1	00	0	0	0	0	-	
			...	Repeat above D Command until 2* nFAW + 2* nRRD - 1														
		12	2*nFAW+2*nRRD	repeat Sub-Loop 10, but BA[2:0] = 2														
		13	2*nFAW+3*nRRD	repeat Sub-Loop 11, but BA[2:0] = 3														
		14	2*nFAW+4*nRRD	D	1	0	0	0	0	0	3	00	0	0	0	0	-	
				Assert and repeat above D Command until 3* nFAW - 1, if necessary														
		15	3*nFAW	repeat Sub-Loop 10, but BA[2:0] = 4														
		16	3*nFAW+nRRD	repeat Sub-Loop 11, but BA[2:0] = 5														
		17	3*nFAW+2*nRRD	repeat Sub-Loop 10, but BA[2:0] = 6														
18	3*nFAW+3*nRRD	repeat Sub-Loop 11, but BA[2:0] = 7																
19	3*nFAW+4*nRRD	D	1	0	0	0	0	0	7	00	0	0	0	0	-			
		Assert and repeat above D Command until 4* nFAW - 1, if necessary																

 a) DM must be driven LOW all the time. DQS,  $\overline{DQS}$  are used according to RD Commands, otherwise MID-LEVEL.

b) Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are MID-LEVEL.



## IDD Specifications

IDD values are for full operating range of voltage and temperature unless otherwise noted.

### $I_{DD}$ Specification

Speed Grade Bin	DDR3L - 1066 7-7-7	DDR3L - 1333 9-9-9	DDR3L - 1600 11-11-11	DDR3L - 1866 13-13-13	Unit	Notes
Symbol	Max.	Max.	Max.	Max.		
$I_{DD0}$	32	35	40	45	mA	x8
	42	44	46	48	mA	x16
$I_{DD1}$	40	46	54	58	mA	x8
	55	58	60	62	mA	x16
$I_{DD2N}$	16	18	20	22	mA	x8
	18	20	22	24	mA	x16
$I_{DD2NT}$	20	22	24	26	mA	x8
	22	26	28	30	mA	x16
$I_{DD2P0}$	12	12	12	12	mA	x8/x16
$I_{DD2P1}$	15	15	15	18	mA	x8/x16
$I_{DD2Q}$	18	18	20	20	mA	x8
	18	20	22	24	mA	x16
$I_{DD3N}$	18	20	22	24	mA	x8
	32	35	35	38	mA	x16
$I_{DD3P}$	10	10	12	12	mA	x8
	20	22	22	24	mA	x16
$I_{DD4R}$	65	80	90	100	mA	x8
	108	125	145	165	mA	x16
$I_{DD4W}$	60	68	80	90	mA	x8
	100	115	130	145	mA	x16
$I_{DD5B}$	75	75	80	85	mA	x8
	100	100	105	110	mA	x16
$I_{DD6}$	12	12	12	12	mA	x8/x16
$I_{DD6ET}$	15	15	15	15	mA	x8/x16
$I_{DD6}$ Low Power	5	5	5	5	mA	x8/x16
$I_{DD7}$	125	150	175	205	mA	x8
	196	198	208	225	mA	x16

#### Notes:

1. Applicable for MR2 settings A6=0 and A7=0. Temperature range for IDD6 is 0 - 85°C.
2. Applicable for MR2 settings A6=0 and A7=1. Temperature range for IDD6ET is 0 - 95°C.

## Input/Output Capacitance

Parameter	Symbol	DDR3L-1066		DDR3L-1333		DDR3L-1600		DDR3L-1866		Unit s	Note s
		Min	Max	Min	Max	Min	Max	Min	Max		
Input/output capacitance (DQ, DM, DQS, $\overline{DQS}$ , TDQS, $\overline{TDQS}$ )	$C_{IO}$	1.5	2.7	1.5	2.5	1.5	2.3	1.4	2.2	pF	1,2,3
Input capacitance, CK and $\overline{CK}$	$C_{CK}$	0.8	1.6	0.8	1.4	0.8	1.4	0.8	1.3	pF	2,3
Input capacitance delta CK and $\overline{CK}$	$C_{DCK}$	0	0.15	0	0.15	0	0.15	0	0.15	pF	2,3,4
Input capacitance delta, DQS and $\overline{DQS}$	$C_{DDQS}$	0	0.20	0	0.15	0	0.15	0	0.15	pF	2,3,5
Input capacitance (All other input-only pins)	$C_I$	0.75	1.35	0.75	1.3	0.75	1.3	0.75	1.2	pF	2,3,6
Input capacitance delta (All CTRL input-only pins)	$C_{DI\_CTRL}$	-0.5	0.3	-0.4	0.2	-0.4	0.2	-0.4	0.2	pF	2,3,7,8
Input capacitance delta (All ADD/CMD input-only pins)	$C_{DI\_ADD\_CMD}$	-0.5	0.5	-0.4	0.4	-0.4	0.4	-0.4	0.4	pF	2,3,9,10
Input/output capacitance delta (DQ, DM, DQS, $\overline{DQS}$ )	$C_{DIO}$	-0.5	0.3	-0.5	0.3	-0.5	0.3	-0.5	0.3	pF	2,3,11
Input/output capacitance of ZQ pin	$C_{ZQ}$	-	3	-	3	-	3	-	3	pF	2,3,12

### Notes:

1. Although the DM, TDQS and  $\overline{TDQS}$  pins have different functions, the loading matches DQ and DQS.
2. This parameter is not subject to production test. It is verified by design and characterization. The capacitance is measured according to JEP147("PROCEDURE FOR MEASURING INPUT CAPACITANCE USING A VECTOR NETWORK ANALYZER(VNA)") with VDD, VDDQ, VSS, VSSQ applied and all other pins floating (except the pin under test, CKE,  $\overline{RESET}$  and ODT as necessary). VDD=VDDQ=1.5V, VBIAS=VDD/2 and on-die termination off.
3. This parameter applies to monolithic devices only; stacked/dual-die devices are not covered here
4. Absolute value of  $C_{CK}-C_{\overline{CK}}$ .
5. Absolute value of  $C_{IO}(DQS)-C_{IO}(\overline{DQS})$ .
6.  $C_I$  applies to ODT,  $\overline{CS}$ , CKE, A0-A15, BA0-BA2,  $\overline{RAS}$ ,  $\overline{CAS}$ ,  $\overline{WE}$ .
7.  $C_{DI\_CTR}$  applies to ODT,  $\overline{CS}$  and CKE.
8.  $C_{DI\_CTRL}=C_I(CNTL) - 0.5 * C_I(CLK) + C_I(\overline{CLK})$
9.  $C_{DI\_ADD\_CMD}$  applies to A0-A15, BA0-BA2,  $\overline{RAS}$ ,  $\overline{CAS}$  and  $\overline{WE}$ .
10.  $C_{DI\_ADD\_CMD}=C_I(ADD\_CMD) - 0.5*(C_I(CLK)+C_I(\overline{CLK}))$
11.  $C_{DIO}=C_{IO}(DQ) - 0.5*(C_{IO}(DQS)+C_{IO}(\overline{DQS}))$
12. Maximum external load capacitance an ZQ pin: 5 pF.

## Standard Speed Bins

DDR3L SDRAM Standard Speed Bins include tCK, tRCD, tRP, tRAS and tRC for each corresponding bin.

## DDRL3-1066 Speed Bins

For specific Notes see "Speed Bin Table Notes" on page 31.

Speed Bin		DDR3L-1066 G7		Unit	Note	
CL - nRCD - nRP		7-7-7				
Parameter	Symbol	min	max			
Internal read command to first data	$t_{AA}$	13.125	20	ns		
ACT to internal read or write delay time	$t_{RCD}$	13.125	—	ns		
PRE command period	$t_{RP}$	13.125	—	ns		
ACT to ACT or REF command period	$t_{RC}$	50.625	—	ns		
ACT to PRE command period	$t_{RAS}$	37.5	9 * tREFI	ns		
CL = 5	CWL = 5	$t_{CK(AVG)}$	3.0	3.3	ns	1,2,3,4,6,10,11
	CWL = 6	$t_{CK(AVG)}$	Reserved		ns	4
CL = 6	CWL = 5	$t_{CK(AVG)}$	2.5	3.3	ns	1,2,3,6
	CWL = 6	$t_{CK(AVG)}$	Reserved		ns	1,2,3,4
CL = 7	CWL = 5	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5	ns	1,2,3,4
CL = 8	CWL = 5	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5	ns	1,2,3
Supported CL Settings		5, 6, 7, 8		$n_{CK}$	13	
Supported CWL Settings		5, 6		$n_{CK}$		

## DDR3L-1333 Speed Bins

For specific Notes see "Speed Bin Table Notes" on page 31.

Speed Bin		DDR3L-1333 H9		Unit	Note	
CL - nRCD - nRP		9-9-9				
Parameter	Symbol	min	max			
Internal read command to first data	$t_{AA}$	13.5 (13.125) <sup>11</sup>	20	ns		
ACT to internal read or write delay time	$t_{RCD}$	13.5 (13.125) <sup>11</sup>	—	ns		
PRE command period	$t_{RP}$	13.5 (13.125) <sup>11</sup>	—	ns		
ACT to ACT or REF command period	$t_{RC}$	49.5 (49.125) <sup>11</sup>	—	ns		
ACT to PRE command period	$t_{RAS}$	36	9 * tREFI	ns		
CL = 5	CWL = 5	$t_{CK(AVG)}$	3.0	3.3	ns	1,2,3,4,7,10,11
	CWL = 6, 7	$t_{CK(AVG)}$	Reserved		ns	4
CL = 6	CWL = 5	$t_{CK(AVG)}$	2.5	3.3	ns	1,2,3,7
	CWL = 6	$t_{CK(AVG)}$	Reserved		ns	1,2,3,4,7
	CWL = 7	$t_{CK(AVG)}$	Reserved		ns	4
CL = 7	CWL = 5	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5	ns	1,2,3,4,7
			(Optional) Note 5,11			
CWL = 7	$t_{CK(AVG)}$	Reserved		ns	1,2,3,4	
CL = 8	CWL = 5	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5	ns	1,2,3,7
	CWL = 7	$t_{CK(AVG)}$	Reserved		ns	1,2,3,4
CL = 9	CWL = 5, 6	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 7	$t_{CK(AVG)}$	1.5	<1.875	ns	1,2,3,4
CL = 10	CWL = 5, 6	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 7	$t_{CK(AVG)}$	1.5	<1.875	ns	1,2,3
			(Optional)		ns	5
Supported CL Settings		5,6,(7),9,(10)		$n_{CK}$		
Supported CWL Settings		5, 6, 7		$n_{CK}$		

## DDR3L-1600 Speed Bins

For specific Notes see "Speed Bin Table Notes" on page 31.

Speed Bin		DDR3L-1600 PB		Unit	Note	
CL - nRCD - nRP		11-11-11				
Parameter	Symbol	min	max			
Internal read command to first data	$t_{AA}$	13.75 (13.125) <sup>11</sup>	20	ns		
ACT to internal read or write delay time	$t_{RCD}$	13.75 (13.125) <sup>11</sup>	—	ns		
PRE command period	$t_{RP}$	13.75 (13.125) <sup>11</sup>	—	ns		
ACT to ACT or REF command period	$t_{RC}$	48.75 (48.125) <sup>11</sup>	—	ns		
ACT to PRE command period	$t_{RAS}$	35	9 * tREFI	ns		
CL = 5	CWL = 5	$t_{CK(AVG)}$	3.0	3.3	ns	1,2,3,4,8, 10,11
	CWL = 6, 7, 8	$t_{CK(AVG)}$	Reserved		ns	4
CL = 6	CWL = 5	$t_{CK(AVG)}$	2.5	3.3	ns	1,2,3,8
	CWL = 6	$t_{CK(AVG)}$	Reserved		ns	1,2,3,4,8
	CWL = 7, 8	$t_{CK(AVG)}$	Reserved		ns	4
CL = 7	CWL = 5	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5	ns	1,2,3,4,8
			(Optional) Note 5,11			
	CWL = 7	$t_{CK(AVG)}$	Reserved		ns	1,2,3,4,8
CWL = 8	$t_{CK(AVG)}$	Reserved		ns	4	
CL = 8	CWL = 5	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5	ns	1,2,3,8
	CWL = 7	$t_{CK(AVG)}$	Reserved		ns	1,2,3,4,8
	CWL = 8	$t_{CK(AVG)}$	Reserved		ns	1,2,3,4
CL = 9	CWL = 5, 6	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 7	$t_{CK(AVG)}$	1.5	<1.875	ns	1,2,3,4,8
			(Optional) Note 5,11			
CWL = 8	$t_{CK(AVG)}$	Reserved		ns	1,2,3,4	
CL = 10	CWL = 5, 6	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 7	$t_{CK(AVG)}$	1.5	<1.875	ns	1,2,3,8
	CWL = 8	$t_{CK(AVG)}$	Reserved		ns	1,2,3,4
CL = 11	CWL = 5, 6,7	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 8	$t_{CK(AVG)}$	1.25	<1.5	ns	1,2,3
Supported CL Settings		5,6,(7),8,(9),10,11		$n_{CK}$		
Supported CWL Settings		5, 6, 7, 8		$n_{CK}$		

## DDR3L-1866 Speed Bins

For specific Notes See "Speed Bin Table Notes" on page 31.

Speed Bin		DDR3L-1866 RD		Unit	Note	
CL - nRCD - nRP		13-13-13				
Parameter	Symbol	min	max			
Internal read command to first data	$t_{AA}$	13.91(13.125) (Optional Note 5,11)	20	ns		
ACT to internal read or write delay time	$t_{RCD}$	13.91(13.125) (Optional Note 5,11)	—	ns		
PRE command period	$t_{RP}$	13.91(13.125) (Optional Note 5,11)	—	ns		
ACT to PRE command period	$t_{RAS}$	34	9 * tREFI	ns		
ACT to ACT or PRE command period	$t_{RC}$	47.91(47.125) (Optional Note 5,11)	-	ns		
CL = 5	CWL = 5	$t_{CK(AVG)}$	Reserved	ns	1, 2, 3, 4, 9	
	CWL = 6,7,8,9	$t_{CK(AVG)}$	Reserved	ns	4	
CL = 6	CWL = 5	$t_{CK(AVG)}$	2.5	3.3	ns	1, 2, 3, 9
	CWL = 6	$t_{CK(AVG)}$	Reserved		ns	1, 2, 3, 4, 9
	CWL = 7,8,9	$t_{CK(AVG)}$	Reserved		ns	4
CL = 7	CWL = 5	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 6	$t_{CK(AVG)}$	1.875 (Optional)	< 2.5 (Optional)	ns	1, 2, 3, 4, 9,11
	CWL = 7,8,9	$t_{CK(AVG)}$	Reserved		ns	4
CL = 8	CWL = 5	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5	ns	1, 2, 3, 9
	CWL = 7	$t_{CK(AVG)}$	Reserved		ns	1, 2, 3, 4, 9
	CWL = 8,9	$t_{CK(AVG)}$	Reserved		ns	4
CL = 9	CWL = 5, 6	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 7	$t_{CK(AVG)}$	1.5 (Optional)	<1.875 (Optional)	ns	1, 2, 3, 4, 9,11
	CWL = 8	$t_{CK(AVG)}$	Reserved		ns	1, 2, 3, 4, 9
	CWL = 9	$t_{CK(AVG)}$	Reserved		ns	4
CL = 10	CWL = 5, 6	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 7	$t_{CK(AVG)}$	1.5	<1.875	ns	1, 2, 3, 9
	CWL = 8	$t_{CK(AVG)}$	Reserved		ns	1, 2, 3, 4, 9
CL = 11	CWL = 5,6,7	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 8	$t_{CK(AVG)}$	1.25 (Optional)	<1.5 (Optional)	ns	1, 2, 3, 4, 9,11
	CWL = 9	$t_{CK(AVG)}$	Reserved		ns	1, 2, 3, 4
CL = 12	CWL = 5,6,7,8	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 9	$t_{CK(AVG)}$	Reserved		ns	1,2,3,4
CL = 13	CWL = 5,6,7,8	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 9	$t_{CK(AVG)}$	1.07	<1.25	ns	1, 2, 3
Supported CL Settings		6, (7), 8, (9), 10, (11), 13		$n_{CK}$		
Supported CWL Settings		5, 6, 7, 8, 9		$n_{CK}$		

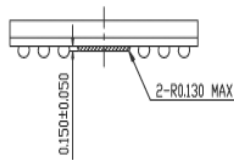
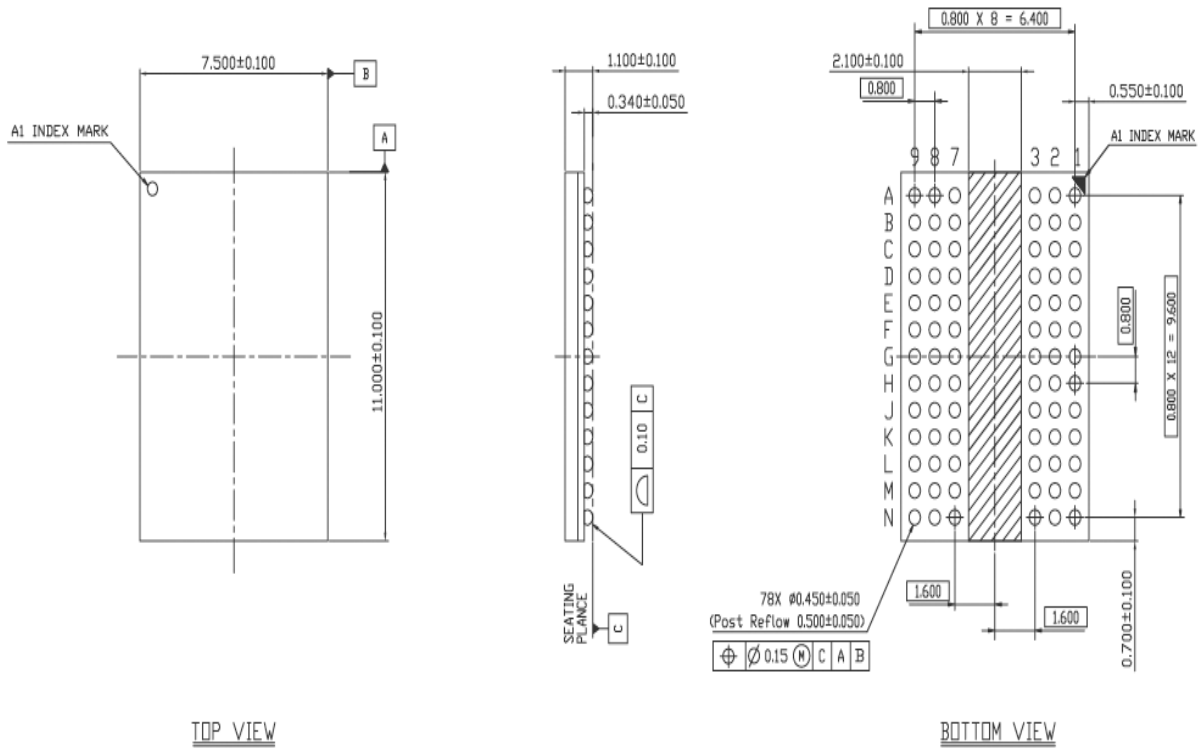
## Speed Bin Table Notes

Absolute Specification ( $T_{OPER}$ ;  $V_{DDQ} = V_{DD} = 1.5V \pm 0.075 V$ );

1. The CL setting and CWL setting result in  $t_{CK(AVG).MIN}$  and  $t_{CK(AVG).MAX}$  requirements. When making a selection of  $t_{CK(AVG)}$ , both need to be fulfilled: Requirements from CL setting as well as requirements from CWL setting.
2.  $t_{CK(AVG).MIN}$  limits: Since CAS Latency is not purely analog - data and strobe output are synchronized by the DLL - all possible intermediate frequencies may not be guaranteed. An application should use the next smaller JEDEC standard  $t_{CK(AVG)}$  value (3.0, 2.5, 1.875, 1.5, or 1.25 ns) when calculating  $CL [nCK] = t_{AA} [ns] / t_{CK(AVG)} [ns]$ , rounding up to the next 'Supported CL', where  $t_{CK(AVG)} = 3.0$  ns should only be used for  $CL = 5$  calculation.
3.  $t_{CK(AVG).MAX}$  limits: Calculate  $t_{CK(AVG)} = t_{AA}.MAX / CL$  SELECTED and round the resulting  $t_{CK(AVG)}$  down to the next valid speed bin (i.e. 3.3ns or 2.5ns or 1.875 ns or 1.25 ns). This result is  $t_{CK(AVG).MAX}$  corresponding to CL SELECTED.
4. 'Reserved' settings are not allowed. User must program a different value.
5. 'Optional' settings allow certain devices in the industry to support this setting, however, it is not a mandatory feature. Refer to SK hynix Inc. DIMM data sheet and/or the DIMM SPD information if and how this setting is supported.
6. Any DDR3-1066 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
7. Any DDR3-1333 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
8. Any DDR3-1600 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
9. Any DDR3-1866 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
10. Any DDR3-2133 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
11. SK hynix Inc. DDR3 SDRAM devices supporting optional down binning to  $CL=7$ ,  $9$  and  $CL=11$ , and  $t_{AA}/t_{RCD}/t_{RP}$  must be 13.125 ns. SPD settings must be programmed to match. For example, DDR3-1866 RD devices supporting down binning to DDR3-1600K or DDR3-1333 H9 or 1066 G7 should program 13.125 ns in SPD bytes for  $t_{AAmin}$  (Byte 16),  $t_{RCDmin}$  (Byte 18), and  $t_{RPmin}$  (Byte 20). Once  $t_{RP}$  (Byte 20) is programmed to 13.125ns,  $t_{RCmin}$  (Byte 21,23) also should be programmed accordingly. For example, 49.125ns ( $t_{RASmin} + t_{RPmin} = 36$  ns + 13.125 ns) for DDR3-1333 H9 and 48.125ns ( $t_{RASmin} + t_{RPmin} = 35$  ns + 13.125 ns) for DDR3-1600 PB.
12. For CL5 support, refer to DIMM SPD information. DRAM is required to support CL5. CL5 is not mandatory in SPD coding.

## Package Dimensions

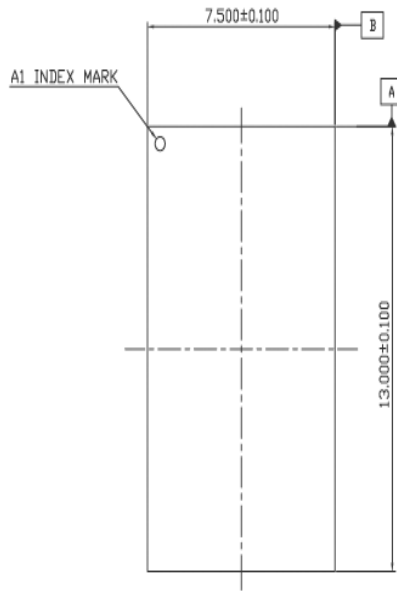
### Package Dimension(x8): 78Ball Fine Pitch Ball Grid Array Outline



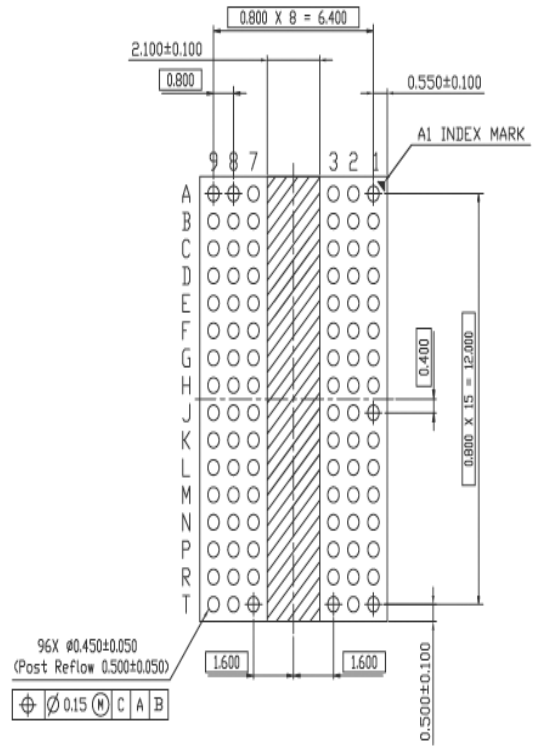
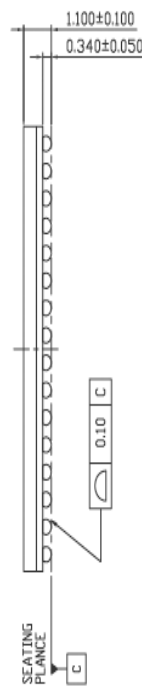
FRONT VIEW



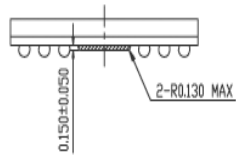
## Package Dimension(x16): 96Ball Fine Pitch Ball Grid Array Outline



TOP VIEW



BOTTOM VIEW



FRONT VIEW